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DRIFT TRACKING FEEDBACK FOR COMMUNICATION CHANNELS

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BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to the calibration of communication channel parameters in systems, including mesochronous systems, in which two (or more) components communicate via an interconnection link; and to the calibration needed to account for drift of conditions related to such parameters during operation of the communication channels.

Description of Related Art

[0002] In high-speed communication channels, including channels which are operated in a mesochronous manner, a transmitter and receiver are each locked to a specific phase relative to some global reference clock. The phase values of the transmitter and receiver which minimize the bit-error-rate of the communication channel may be determined in a number of ways. However, once these phase values are set, offsets due to system conditions (such as temperature effects on the propagation time of the wires in the link) will cause the chosen phase values to become non-optimal. Other parameters of the communication channel also drift due to changing system conditions.

[0003] It is therefore desirable to provide techniques to detect and compensate for the drift in parameters of a communication channel due to changing system conditions like these.

SUMMARY OF THE INVENTION

[0004] The present invention provides a system and method for setting a parameter of a communication channel, which allows for optimizing the parameter while efficiently tracking drift of properties of the channel. A communication channel includes a first component having a transmitter coupled to a normal signal source, and a second component having a receiver coupled to a normal signal destination. A communication

link couples the first and second components. The communication system provides for setting an operation value for the parameter, which for example can include executing an exhaustive calibration sequence at initialization of the channel. The method and system of the present invention provides for tracking drift in the parameter by monitoring a signal on another channel that is characterized by drift relative to a reference, such as a reference clock, in amounts that correlate with drift in the parameter of communication channel relative to the reference, and to update, or indicate the need for updating, the operation value of the parameter in response to the monitoring function. The signal being monitored is provided in various ways according to embodiments of the invention, including by signals on channels that emulate the channel being monitored, by signals on another channel within a single communication bus, by signals on a channel that loops back to a component on the channel that generates it, or by signals that otherwise exhibit characteristics that correlate, whether causally or not, to the parameter being tracked on the channel.

[0005] In embodiments of the invention, the parameter is updated by executing a calibration sequence on the communication link. In other embodiments, the updating includes adjusting the operation value of the parameter as a function of the drift determined by monitoring the signal.

[0006] According to embodiments of the present invention, the parameter of the communication channel is the phase of one of the receive and transmit clocks for an input/output driver, where the phase establishes a sample timing point for a receiver, or a drive timing point for a transmitter. The monitoring function operates by comparing the phase of the signal with the phase of a reference clock. Because the signal being monitored drifts in phase by amounts that correlate with the drift in phase of the sample timing point or drive timing point of communication channel being adjusted, the relative phase changes can be relied upon to indicate the need for updating the operation value of the parameter.

[0007] The signal being monitored in order to track drift in various embodiments comprises a data transmission signal, for example, on another communication channel. The monitoring step, in some embodiments, includes detecting transitions in the data transmission, and comparing the detected transitions with transitions in the reference

clock. In other embodiments, the monitored signal comprises a control signal used for controlling communications in the communication channel, such as a data strobe between the components using the communication channel. In yet other embodiments, the monitored signal comprises a signal taken from outside the communication channel that nonetheless can be relied upon for emulating drift in the parameter.

[0008] The invention is also embodied by an apparatus coupled with a driver for a communication channel. The apparatus includes memory to store the operation value of the parameter, logic to monitor a signal which has a characteristic that correlates with the parameter of the communication channel to track drift in the characteristic, and logic to indicate the need to update, or to update directly, the operation value based on the drift in the monitored signal.

[0009] An embodiment of the present invention comprises an interface for a communication bus. The interface includes a plurality of input/output drivers coupled with respective bidirectional links in the communication bus. The input/output drivers include a transmitter responsive to a transmit clock, which drives a signal on a corresponding link in the communication bus. Also, a receiver is included in the input/output driver, that is responsive to a receive clock. The receiver samples a signal on the corresponding link. A transmit clock generator and a receive clock generator are coupled respectively to the transmitter and the receiver, and to a reference clock. At least one of the transmit clock generator and the receive clock generator is adjustable in response to a phase control signal. The interface also includes a drift tracking circuit. The drift tracking circuit is coupled to a link carrying a monitored signal that is characterized by drift that correlates with drift in the communication bus. The drift tracking circuit includes a tracking clock generator that is coupled to the reference clock and generates a tracking clock. A phase detector is included in the drift tracking circuit, to track changes in phase between the tracking clock and transitions in the monitored signal. Logic in the drift tracking circuit monitors the changes in phase, and issues an indication that the phase control signal be updated to account for the changes in phase.

[0010] The receive clock generator and the transmit clock generator in some embodiments of the interface comprise a phase locked loop, coupled to the reference clock, which produces a set of output clocks that are some multiple of the input reference

frequency. A mixer is coupled with the phase locked loop, and is responsive to the phase control signal to generate the transmit or receive clock, having an adjustable phase as indicated by the phase control signal. Also, memory coupled with the clock generator stores the phase control signal.

[0011] In yet other embodiments of the interface, calibration logic is included to determine the operation value of the phase control signal. The calibration logic is responsive to the indication from the drift tracking circuit, to re-calibrate the operation value of the phase control signal. Also, the calibration logic may be executed to initially set the operation value of the phase control signal, for example at start up of the interface.

[0012] Accordingly, the present invention provides for drift tracking based on data collected during normal operation of a communication channel, without relying upon periodic calibration sequences that remove the communication channel from its mission function. Thus, the present invention tracks drift of parameters of the communication channel, including mesochronous channels, while preserving overall throughput and latency characteristics of the link. The present invention is particularly suited to high speed communication channels, including chip-to-chip channels with links across traces on printed circuit boards, or other board level media, operating with system clocks over 100 MegaHertz, including clocks with frequencies in the range of 400 MegaHertz, and higher.

[0013] Other aspects and advantages of the present invention can be seen on review of the drawings, the detailed description and the claims, which follow.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] Fig. 1 is a simplified diagram of two components interconnected by a communication channel, with drift tracking according to an embodiment of the present invention.

[0015] Fig. 2 is a simplified diagram of two components interconnected by a communication channel, with drift tracking according to another embodiment of the present invention.

[0016] Fig. 3 illustrates an embodiment of an interface to a communication channel, including input/output drivers and a drift tracking circuit according to the present invention.

[0017] Fig. 4 is a flow chart of operation of calibration logic used to set the operation value of the parameter of the communication channel in some embodiments of the present invention.

[0018] Fig. 5 illustrates an embodiment of an interface to a communication channel between a memory controller and a memory, such as a DRAM, including input/output drivers and a drift tracking circuit according to the present invention with data strobe monitoring.

[0019] Fig. 6 illustrates an embodiment of an interface to a communication channel between first and second chips, including input/output drivers and a drift tracking circuit according to the present invention including a loop back channel carrying a monitored signal.

DETAILED DESCRIPTION

[0020] A detailed description of embodiments of the present invention is provided with reference to the Figures.

[0021] Fig. 1 shows two components 10, 11 connected with an interconnection medium, referred to as link 12. Component 10 has a transmitter circuit 13 which drives symbols (bits) on link 12 in response to timing events on the internal CLKT signal 14. This series of bits forms signal DATAT. Component 11 has a receiver circuit 15 which samples symbols (bits) on link 12 in response to timing events on the internal CLKR signal 16. The DATAT forms signal DATAR at the opposite end of the link, which is sampled by the receiver. The transmit clock CLKT is generated by a transmit clock generator 40. The receive clock CLKR is generated by a receive clock generator 49 that is responsive to a phase control signal stored in a phase calibration register 48. A communication channel between the components 10 and 11 comprises the transmitter circuit 13, the link 12 and the receiver circuit 15. Delay block 50 in the link 12 represents delay encountered in the communication channel, which may drift during operation due to changing operational and environmental conditions in the components and in the link.

For successful data transmission, the relative phases of the transmit clock CLKT and the receive clock CLKR must account for the delay represented by block 50. As the delay represented by block 50 drifts, the relative phases of the transmit clock CLKT and the receive clock CLKR must also be adjusted in order to maintain successful data transmission.

[0022] A tracking circuit 45 on component 11 is coupled to a monitored signal MS on line 46. Line 46 represents a channel, which has a characteristic, such as the drift in phase, which correlates with drift in delay 50 in the communication channel across link 12. The tracking circuit 45 generates an indication on line 47 used to control the value in the phase register 48, which is coupled to the receive clock generator 49. The indication is generated when the drift in the monitored signal on line 46 reaches a predetermined level in some embodiments. In one embodiment, the tracking circuit 45 generates the indication on line 47 on each phase change of the monitored signal, and adjusts the phase control signal in phase register 48 in response to a function of the phase changes indicated by the drift tracking circuit 45. In another alternative, the indication on line 47 is provided to calibration resources, such as special purpose logic, a host processor executing calibration routines, or other resources, which execute a calibration sequence for the link 12 to update the phase control signal in phase register 48.

[0023] In the embodiment of Fig. 1, the tracking circuit is on the receive side of the channel. In alternative embodiments, the tracking circuit is implemented on the transmit side of the channel, or on both the transmit and the receive sides of the channel. Fig. 2 illustrates an embodiment with drift tracking for a parameter of a transmitter in a communication channel between first and second components. Thus, Fig. 2 shows two components 10, 11 connected with an interconnection medium, referred to as link 12. Component 10 has a transmitter circuit 13 which drives symbols (bits) on link 12 in response to timing events on the internal CLKT signal 14. This series of bits forms signal DATAT. Component 11 has a receiver circuit 15 which samples symbols (bits) on link 12 in response to timing events on the internal CLKR signal 16. This series of bits forms signal DATAR. The transmit clock CLKT is generated by a transmit clock generator 40. The receive clock CLKR is generated by a receive clock generator 49. A communication channel between the components 10 and 11 comprises the transmitter

circuit 13, the link 12 and the receiver circuit 15. Delay block 50 in the link 12 represents delay encountered in the communication channel, which may drift during operation due to changing operational and environmental conditions in the components and in the link. For successful data transmission, the relative timing for the communication channel is determined by the phase of the transmit clock CLKT and the phase of the receive clock CLKR. The difference in phase between the two clocks is absorbed by the delay represented by delay block 50.

[0024] A tracking circuit 45 on component 10 is coupled to a monitored signal MS on line 46. Line 46 represents a channel, which has a characteristic such as the drift in phase, that correlates with drift of a parameter in the communication channel across link 12. The tracking circuit 45 generates an indication on line 47 used to control the transmit timing, which is coupled to the transmitter circuit 13. The indication is generated when the drift in the monitored signal on line 46 reaches a predetermined level in some embodiments.

[0025] Fig. 3 illustrates a system including a first integrated circuit 200 and a second integrated circuit 201 which communicate via a communication bus, generally 202. In the system of Fig. 3, a clock generator 250 is included, which provides a reference clock to the master CTM on the first integrated circuit 200. The first integrated circuit 200, in this example provides the reference clock from the master CFM to the second integrated circuit 201.

[0026] The communication bus includes a plurality of communication channels that comprises a transmitter, a communication link and a receiver. For example, the communication bus includes a plurality of bi-directional data links represented by line 203, a plurality of bi-directional address links represented by line 204, and a plurality of bi-directional control links represented by line 205. In other embodiments, the communication bus comprises multidrop links, uni-directional links, or combinations of multidrop, uni-directional and bi-directional links.

[0027] The first integrated circuit 200 and the second integrated circuit 201 include interface circuits supporting the communication bus. For simplicity, an interface circuit for one of the bi-directional data links 203 on the communication bus is shown.

[0028] The interface includes an input/output driver 210. The input/output driver includes a transmitter 211 and a receiver 212. The transmitter 211 accepts input from a normal path used for the mission function of the first integrated circuit 200 and drives the corresponding data on the communication link 203. A transmit clock CLKT is coupled to the transmitter 211 and sets a drive timing point. A receiver (not shown) on the second integrated circuit 201 samples the data from the line 203 in response to a corresponding receive clock. The drive timing point on the transmitter 211 is set by calibration logic 213, using for example a calibration routine as described below, so that the receiver on the second integrated circuit 201 is able to capture correct data.

[0029] Likewise, a receive clock CLKR is coupled to the receiver 212, and sets a sample timing point. The sample timing point is set by the calibration logic 213, in cooperation with a transmitter (not shown) on the second integrated circuit 201 in exemplary embodiments.

[0030] The transmit clock and the receive clock are produced by clock generator circuits. The clock generator circuits include a phase locked loop 214, which produces a set of reference clocks, and supplies those clocks to mixers 215, 216, 217 in the interface. The mixer 215 is used for generating the transmit clock in response to a mixer control signal stored in register 218. The mixer 216 is used for generating the receive clock in response to a mixer control signal stored in register 219. In the illustrated embodiment, registers 218 and 219 are managed by the calibration logic 213. In alternative embodiments, the registers could be managed by higher-layer circuits which implement the equivalent of the calibration logic 213 in software.

[0031] The mixer 217 is used for generating a tracking clock TR-CLK, which is also based on the reference clock CTM so that tracking relative to the tracking clock TR-CLK is, thereby, tracking relative to the reference clock CTM in some embodiments. The tracking clock TR-CLK is supplied to a phase detector 228, which also receives as input a monitored signal from another channel 204 on the communication bus. In this example, the monitored signal is supplied on line 229 from the input to the receiver 227. The phase detector 228 includes a transition detector, so that transitions in the monitored signal and transitions in the tracking clock are utilized for detecting shifts in phase of the monitored signal. The output of the phase detector 228 is supplied to a counter 230,

which counts up and counts down to follow shifts in phase. The output of the counter 230 is used as a phase control signal for the mixer 217. Monitor logic 231 is coupled to the counter 230, and issues indications to the calibration logic 213, in response to changes in the counter value.

[0032] Input/output drivers, like driver 210, are coupled to each of the links in the communication bus. The tracking circuit including the mixer 217, the phase detector 228, and the counter 230, can be repeated for each input/output driver, or shared amongst sets of input/output drivers on the communication bus, or shared among all the links on the bus, depending on level of accuracy needed, the environment of operation for the particular implementation, and other trade-offs.

[0033] The calibration logic 213 may include additional registers, such as registers storing edge values for use during calibration routines as described below, in addition to registers storing the operation value for each of the clocks. The registers 218 and 219 are loaded by the calibration logic 213 depending on the mode of operation.

[0034] Accordingly, the system shown in Fig. 3 performs timing calibration during normal communication between integrated circuits in the system. The calibration of read and write clocks in the integrated circuits may be executed without affecting the normal communication between the integrated circuits. In the embodiment shown, the system includes a clock-data recovery loop which tracks drift by locking itself to an arriving monitored signal, such as read data sent from another integrated circuit device. Based on this clock-data recovery loop, timing correction of the sample clock used to receive data, and the drive timing clock used to transmit data, may be derived.

[0035] According to the present invention, long-term variances in system timing parameters, such as time-of-flight of a data signal, can be detected. Based on this detection, various timing calibration adjustment processes can be initiated. For example, the present invention can be designed so that changes in phase in the tracking circuit of more than a threshold, for example changes of 10 percent, from the state recorded during an initial calibration, result in generation of an indication to the calibration logic that a re-calibration sequence should be executed. Alternatively, when the phase of the tracking clock is shifted by a threshold amount, a compensating adjustment could be made to the phase control values for the input/output driver being monitored.

[0036] Fig. 4 shows calibration steps executed by calibration logic in one exemplary embodiment of the invention, which is suitable for use in combination with the drift tracking circuit described above, in some embodiments to set up initial operation values of the parameters, to periodically update the operation values in response to indications from the drift tracking circuits, or to otherwise supplement the drift tracking circuit.

(Step 301) On initialization, or upon an indication from a drift tracking circuit that a drift measurement is due, suspend transmit and receive operations that are in progress.

(Step 302) Change the sample point of the receiver component from the normal operation value (used for normal operations) to a value used for calibration operations, such as an edge value representing an edge of a timing window for successful reception. It may be necessary to impose a settling delay at this step to allow the new drive point to become stable.

(Step 303) Decouple the transmitter from the normal data path.

(Step 304) Create and transmit a pattern onto the "link." Note that the drive point of the transmitter is fixed relative to the reference clock of the system and is not adjusted.

(Step 305) The pattern set is received in the receive component using the calibration value of the sample point.

(Step 306) The received pattern set is compared to an expected pattern set produced in the receive component. The two pattern sets will either match or not match. As a result of this comparison (and possibly other previous comparisons) a pass or fail determination will be made.

(Step 307) Adjust the sample point operation value in the receiver component as a result of the pass or fail determination.

(Step 308) Repeat steps 302-307 to locate edge values in phase for the sample point outside of which the calibration pattern is not successfully received.

(Step 309) Change the sample point of the receiver to a new operation value (used for normal operations). It may be necessary to impose a settling delay at this step to allow the new drive point to become stable.

(Step 310) Reselect the "normal path" input of the transmitter.

(Step 311) Resume normal transmit and receive operations.

[0037] Fig. 5 illustrates an embodiment of the present invention for a communication channel 203 between a first chip 600 which may be a memory controller as labeled in the drawing, and a second chip 601 which may be a memory like a double data rate DDR dynamic random access memory DRAM as labeled in the drawing, that provides a DQS data strobe signal during read operations. The reference numerals in Fig. 5 are the same as those for components of Fig. 3, with the exception of items relating to the data strobe channel 602. Other components of Fig. 5 are not described again, as they correspond with like numbered components of Fig. 3. In one advantageous embodiment of Fig. 5, the monitored signal for the drift tracking circuit comprises the DQS data strobe control signal produced by the DDR DRAM during read operations (or other data strobe signals or other control signals as appropriate for a particular implementation), and received in data strobe I/O 610 by receiver 603 and provided to read control logic (not shown). The monitor logic 231 is configured to monitor the received read strobe, the transmitted read strobe, or both. When it is configured to track drift from both transmitted read strobes and received read strobes, the logic includes mode control to switch between the two modes. In these embodiments, the monitor function can use shared resources to track drift in the local transmitter, and drift in the combination of the transmission line and the remote transmitter. Of course the shared resource embodiment can be applied to other types of monitored signals.

[0038] Also, the data strobe I/O has calibrated transmit and receive clocks, generated by mixers 604 and 606 respectively, in response to operation value parameters stored in registers 605 and 607.

[0039] Fig. 6 illustrates an embodiment of the present invention for a communication channel 203 between a first chip 200 and a second chip 201, where the monitored signal is provided on a loop back link 650. The reference numerals in Fig. 6 are the same as those for components of Fig. 3, with the exception of the loop back channel including the link 650, the monitored signal transmitter 651, the pattern source 653, and the monitored signal receiver 652. Other components of Fig. 6 are not described again, as they correspond with like numbered components of Fig. 3. In the embodiment shown, a pattern source 653 is coupled to the transmitter 651. The transmitter transmits the pattern, and the receiver receives the looped back pattern. The monitor logic 231 tracks changes

in the phase of the looped back pattern. The pattern source 653 can be replaced by any available signal on the chip 200, such as the CTM reference clock, that has transition density or other characteristics making it suitable for use in tracking drift.

[0040] The link 650 is implemented in some implementations using the same transmission line design as used for the links 203 of the communication channels being adjusted. For example, the chip-to-chip bus is implemented using printed circuit board traces optimized for frequency, length, amplitude of the signal and other parameters. The loop back channel 650 uses the same or similar printed circuit board trace technology, and has a length of for example one-half the average length of the traces forming the channels in the bus, so that the round trip time of flight is close to the time of flight for signals on the bus.

[0041] In one advantageous embodiment of Fig. 6, the loop back channel comprises a transmitter 651 and a link 650 which emulate behavior of the transmitter 211 and link 203 of the communication channel being adjusted. Thus, the looped back signal being monitored from the receiver 652 tracks the behavior of a loop back transmitter 651 on the same chip as the transmitter 211 being adjusted. In other embodiments described above, the transmitter driving the monitored signal is located on a remote chip. Also, in embodiments like that of Fig. 6, the step 301 shown in Fig. 3 may not be necessary during period calibration operations, if the periodic calibration operations are performed using the loop back channel.

[0042] In the embodiments described above, a communication channel is provided having an additional phase mixer, which generates a tracking clock, coupled to a phase detector. The phase detector circuit compares the alignment between the tracking clock and a monitored signal. The monitored signal can consist of either a looped back clock signal, a signal from the memory chip on the opposite end of the communication channel, one of the data bits transmitted on the channel, one of the control bits or address bits transmitted on the channel, or any other signal which correlates with the drift on the communication channel. The tracking circuit, which consists basically of a clock-data recovery control block for systems tracking timing parameters, processes the output of the phase detector and affects adjustments in a counter plus register circuit which controls the phase mixer that generates the tracking clock. A monitor circuit periodically

compares the current value stored in the register, with previous values, and generates outputs based on that comparison. This output can be used simply to indicate that a re-calibration is required, or for real-time adjustment of the operation value of the parameter being monitored.

[0043] According to the present invention, communication systems are provided that track drift, while conserving resources of the communication channels being calibrated. The invention reduces the hardware and storage requirements needed for calibration, reduces the impact on bandwidth and throughput across the communication channel, and maintains accuracy of the operation values of the parameters being calibrated while using less of the resources of the communication channel. Also, the techniques of the present invention improve overall latency characteristics of the communication channel in changing operating conditions.

[0044] While the present invention is disclosed by reference to the preferred embodiments and examples detailed above, it is to be understood that these examples are intended in an illustrative rather than in a limiting sense. It is contemplated that modifications and combinations will readily occur to those skilled in the art, which modifications and combinations will be within the spirit of the invention and the scope of the following claims. What is claimed is: